WHAT IS CLAIMED IS:

1. A power efficiency control (PEC) circuit comprising a plurality of multiplexers (MUXs) having a common input node (IN), an upper output node (UOP) and a lower output node (LOP), wherein the plurality of MUXs are configured to generate output signals at UOP and LOP in response to an input signal at IN such that during an input signal transition at IN, the UOP and the LOP are never on simultaneously.

2. The PEC circuit according to claim 1, wherein the plurality of MUXs is configured to put the UOP and LOP simultaneously in a tri-state condition solely during the input signal transition.

3. The PEC circuit according to claim 1, wherein the output signals at UOP and LOP are CMOS compatible output pre-driver signals.

4. The PEC circuit according to claim 1, wherein the plurality of MUXs are further configured as a pre-driver stage comprising a CMOS UOP pre-driver and a CMOS LOP pre-driver.

5. The PEC circuit according to claim 4, wherein the CMOS UOP pre-driver comprises a PMOS MUX and the CMOS LOP pre-driver comprises an NMOS MUX.

6. The PEC circuit according to claim 1, wherein the plurality of MUXs are further configured such that during an input signal transition at IN, the output signal at UOP and the output signal at LOP reach their final states at different points in time.

7. A power efficiency control (PEC) circuit comprising:

an upper output node (UOP);

a lower output node (LOP);

a common input node (IN); and

means for controlling the UOP and LOP such that during an input signal transition at IN, the UOP and the LOP are never on simultaneously.

8. The PEC circuit according to claim 7, wherein the means for controlling the UOP and LOP comprises a CMOS UOP pre-driver stage and a CMOS LOP pre-driver stage.

9. The PEC circuit according to claim 8, wherein the CMOS UOP pre-driver stage comprises a PMOS multiplexer and the CMOS LOP pre-driver stage comprises an NMOS multiplexer.

10. The PEC circuit according to claim 7, wherein the means for controlling the UOP and LOP is operational to configure both the UOP and LOP to be in a tri-state condition solely during the input signal transition.

11. A method of controlling a CMOS buffer having pull-up and pull-down circuitry, the method comprising the steps of:

providing a multiplexer pre-driver configured to generate a PMOS output signal and an NMOS output signal in response to an input signal;

changing an input signal to the multiplexer pre-driver from a first state to a second state; and

during the changing input signal, operating the multiplexer pre-driver such that both the PMOS output signal and the NMOS output signal are in a tri-state condition simultaneously.

12. The method according to claim 11, wherein during the changing input signal, operating the multiplexer pre-driver further causes the PMOS output signal and the NMOS output signal to reach their final states at different points in time.

13. A power efficiency control (PEC) circuit comprising:

a first multiplexer circuit operational to generate an upper output (UOP) pre-driver signal in response to an input signal; and

a second multiplexer circuit operational to generate a lower output (LOP) pre-driver signal in response to the input signal, wherein the first and second multiplexers are configured such that the UOP pre-driver signal and the LOP pre-driver signal reach their final states at different points in time in response to an input signal transition.

14. The PEC circuit according to claim 13, wherein the first and second multiplexers are further configured such that the UOP pre-driver signal and the LOP pre-driver signal are simultaneously tri-stated during the input signal transition.

15. The PEC circuit according to claim 13, wherein the UOP pre-driver signal is a PMOS signal.

16. The PEC circuit according to claim 13, wherein the LOP pre-driver signal is an NMOS signal.